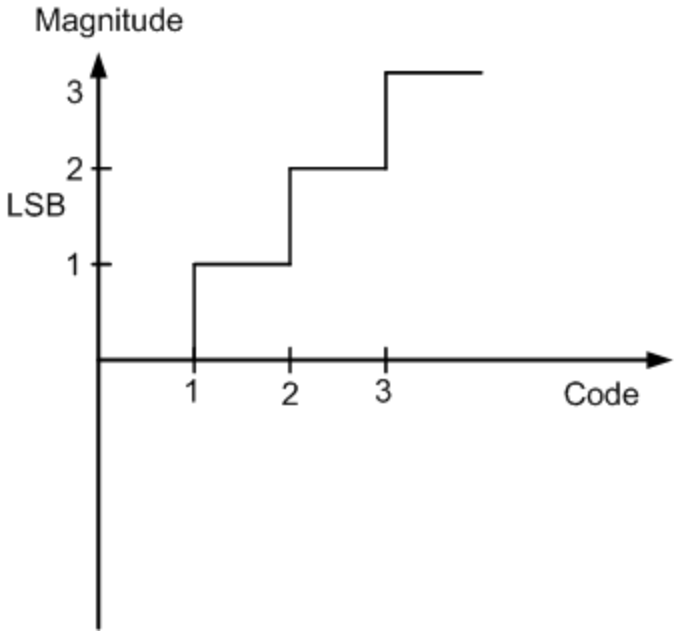
DNL Characteristics

Brian Miller

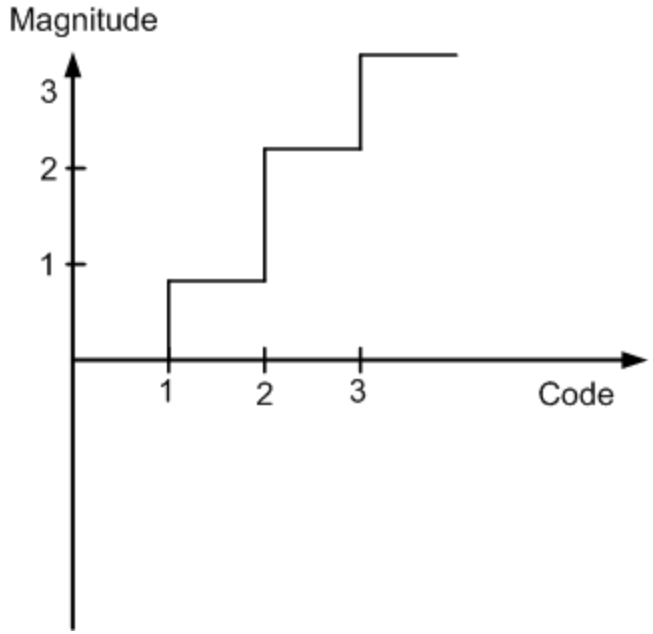
Romesh Nandwana

Differential Non-Linearity (DNL) error

- Amount step size varies from 1LSB



Ideal Case

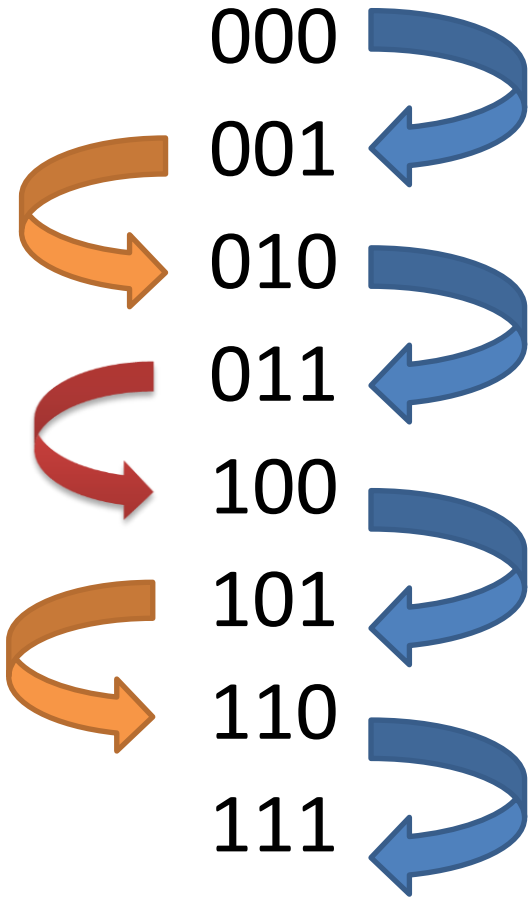


Real Case

Cause of DNL in Current Steering DAC

- DNL in current steering DACs is caused by current mismatches.
- Transistor mismatches largely to blame.
- For a DAC utilizing binary and thermometer code DNL pattern is largely repetitive.

Change In Binary Current Sources



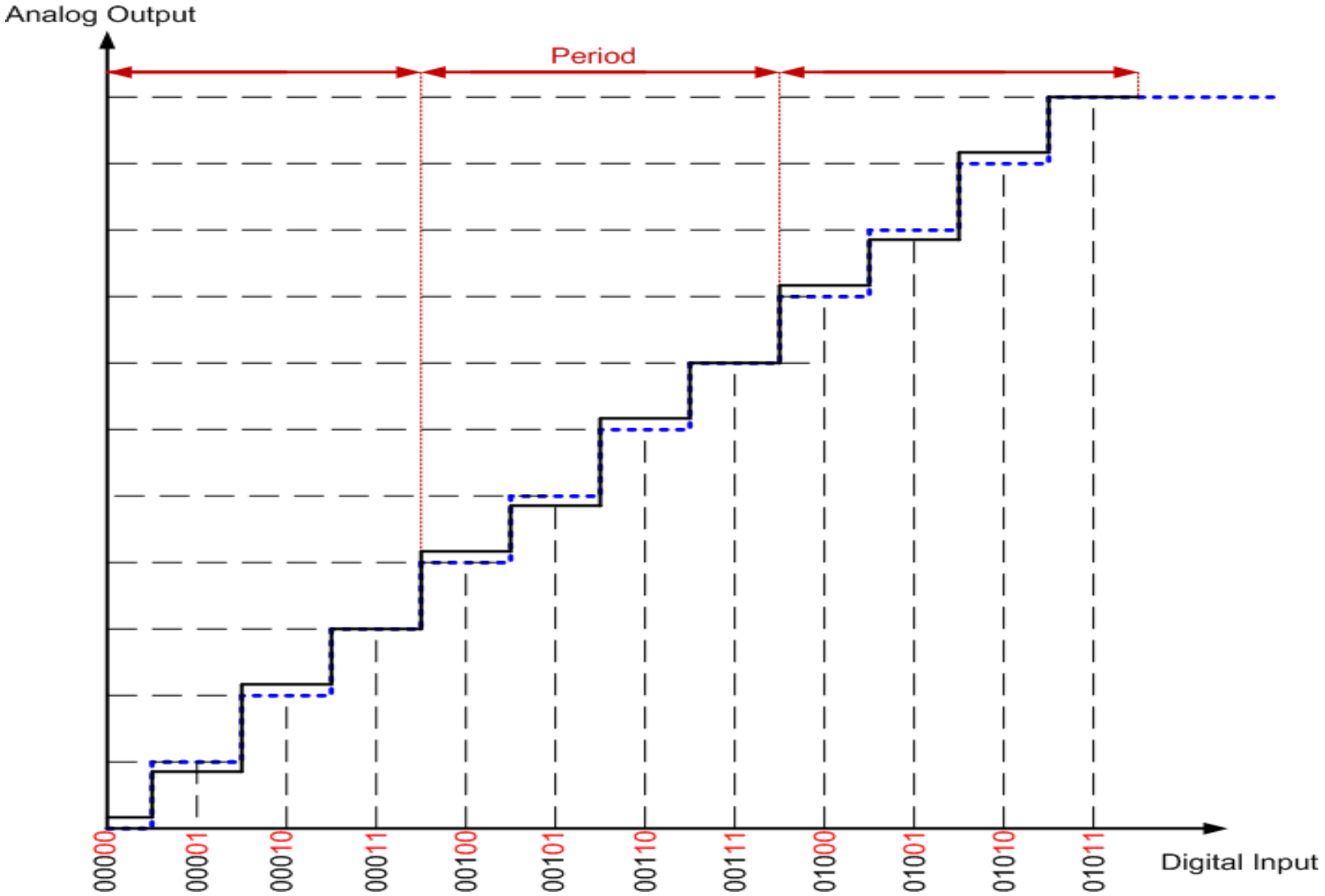
Bit1 on

Bit1 off Bit2 on

Bit 1 & Bit2 off Bit3 on

Periodicity in DNL for Segmented DAC

- Ideal MSB sources

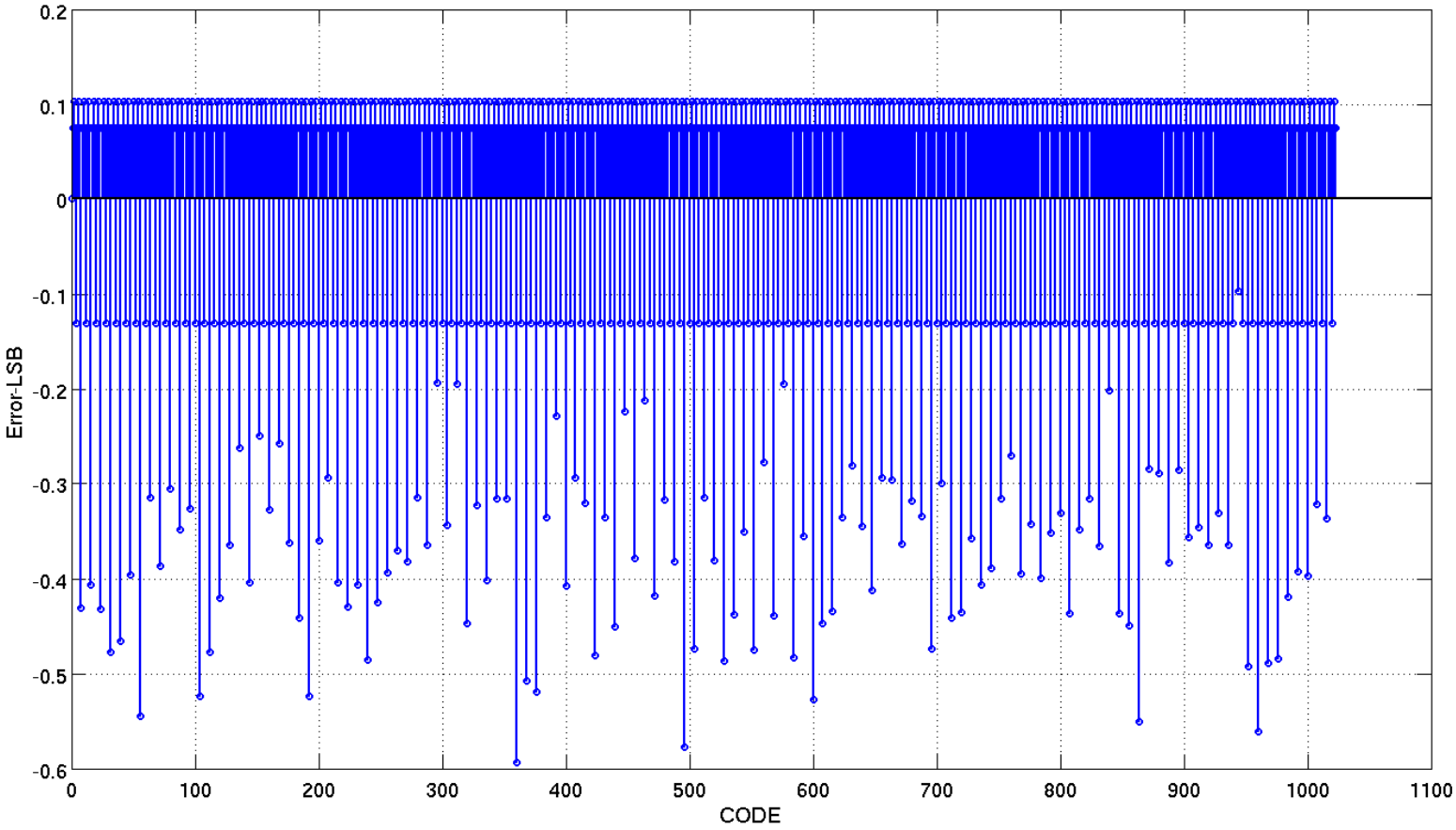


Sum of LSBs determines shape

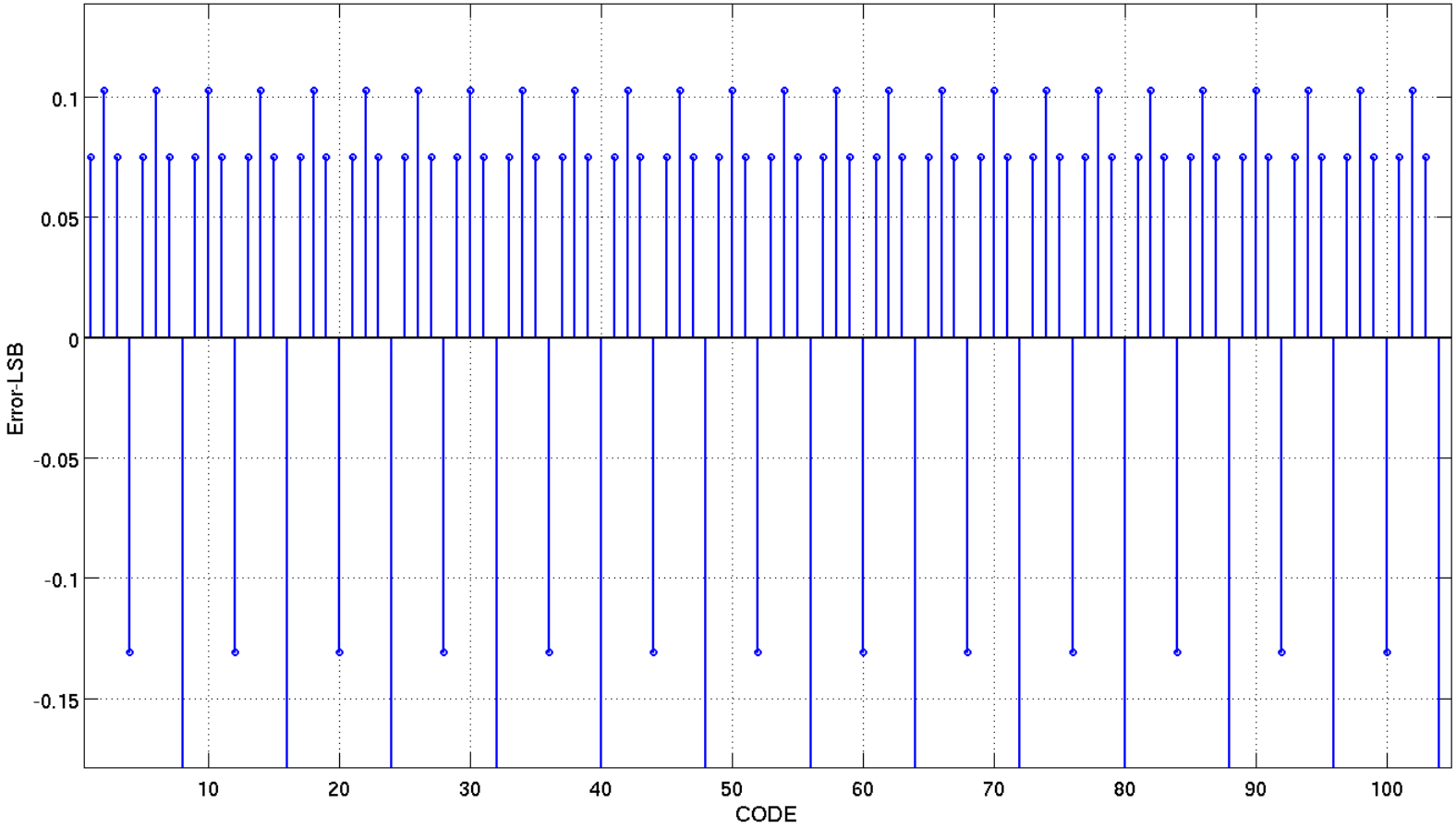
- If sum of LSB currents is much larger than expected, LSBs have DNL larger than zero.
- Random DNL from thermometer code transition will likely have too small of a DNL. A flat top is expected.
- If sum of LSB currents is much smaller than expected, a flat bottom is expected.
- If sum of LSB currents is close to expected then neither a flat top nor flat bottom is expected.

Sum of 3LSB Currents = 7.37LSB

- Nominal Value=7LSB
- Flat top

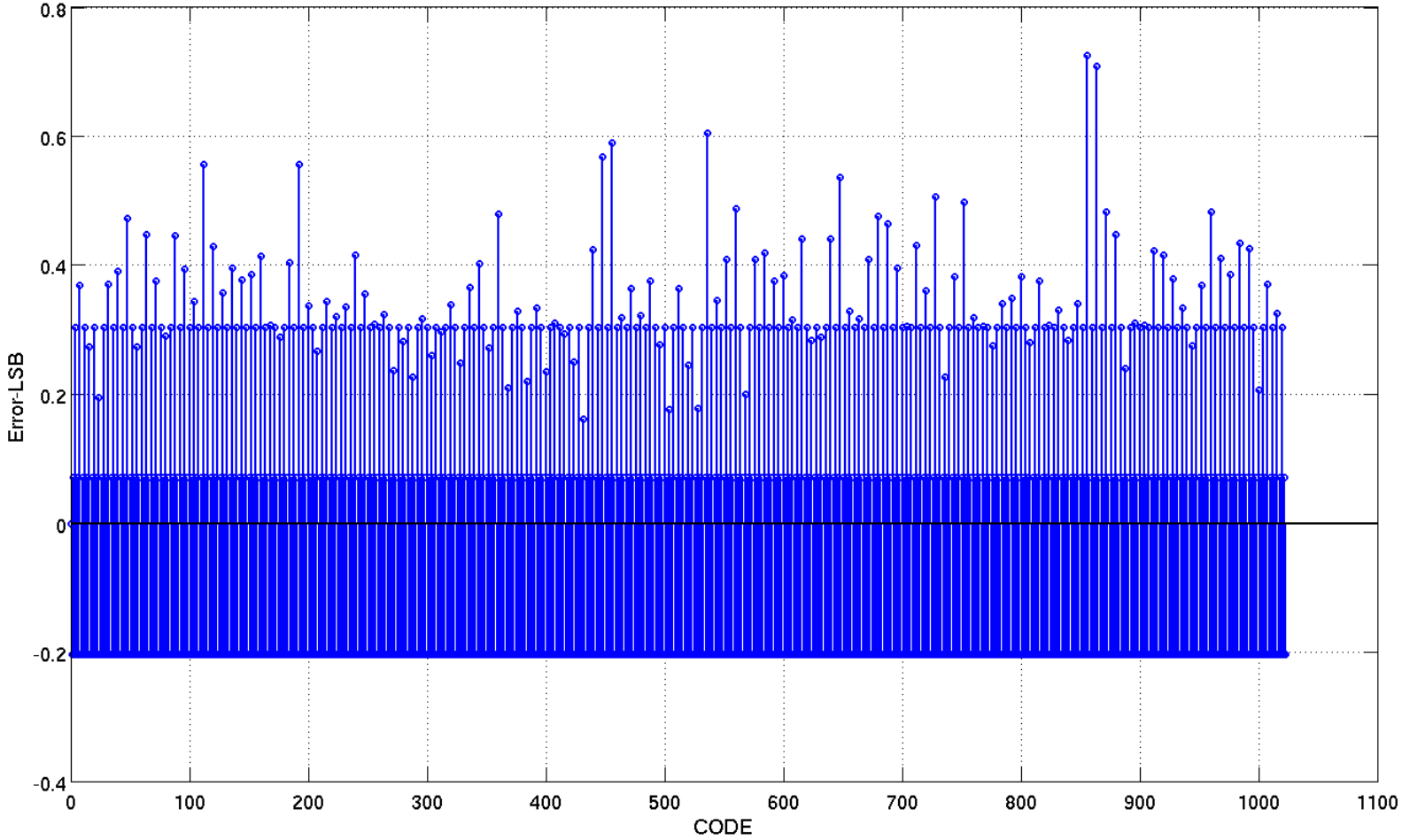


Periodicity



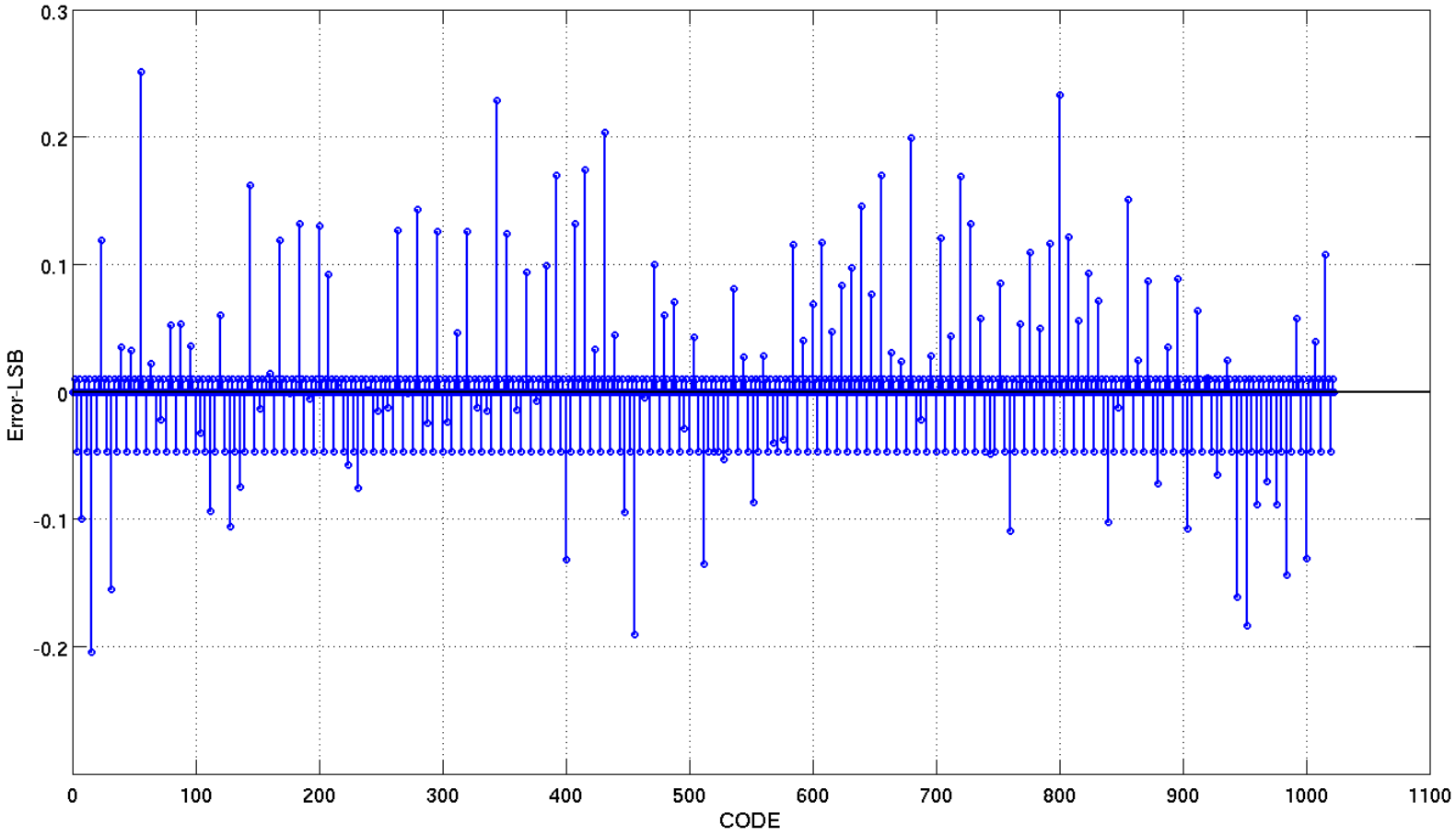
Sum of 3LSBs = 6.63LSB

- Nominal value=7LSB
- Flat bottom



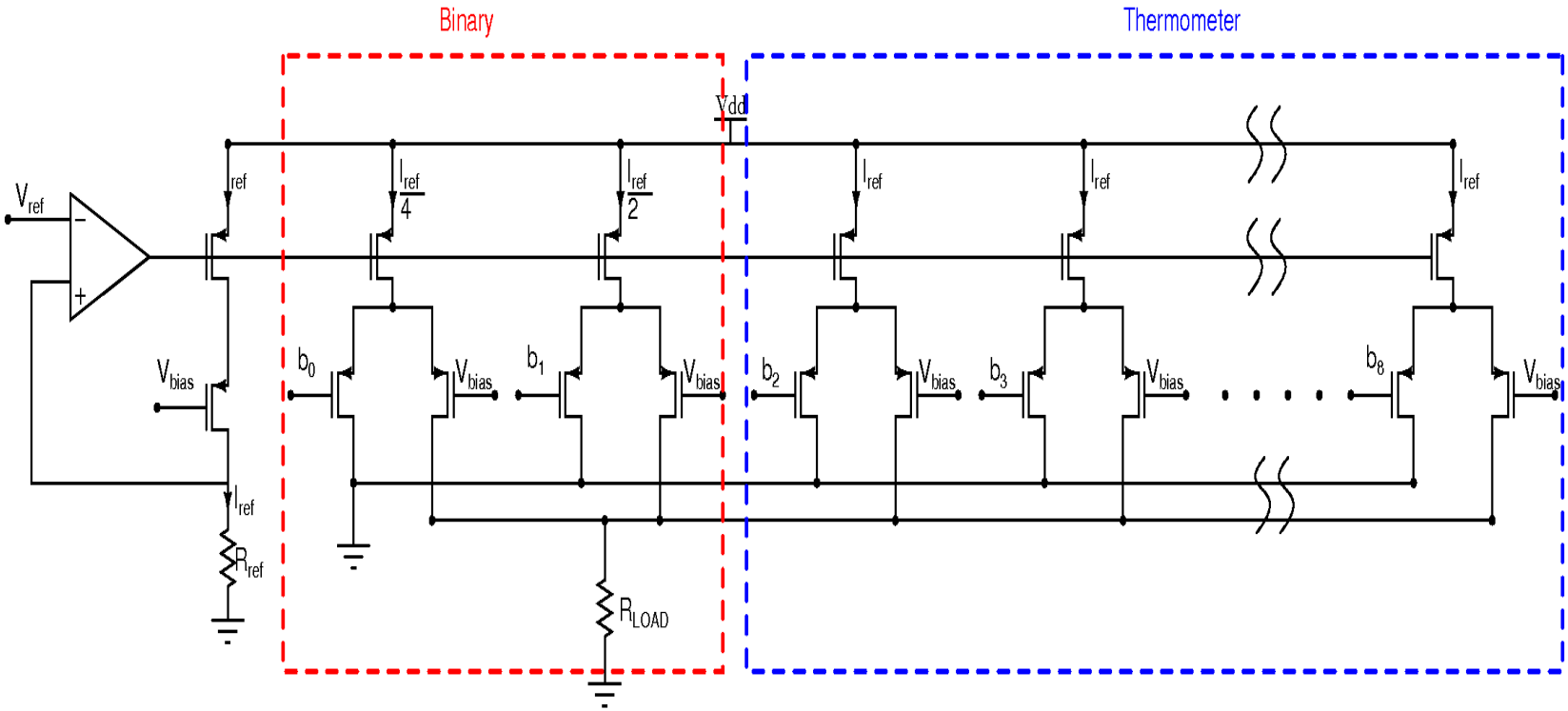
Sum of 3LSBs = 6.97LSB

- Nominal Value=7LSB



Circuit Schematic

- 5bit segmented DAC
- 2 bit binary weighted
- 3 bit thermometer code



Simulated DNL